1as Jornadas de la Red RISC-V

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- **Título de la ponencia:**
  Enhanced Tools for RISC-V Processor Development and Customization

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- **Abstract:**
  The emergence of the RISC-V architecture has given rise to a demand for widely differing microarchitectural implementations, ranging from deeply embedded microcontrollers to DSPs and superscalar processors. To meet the challenge of addressing so many different operating points, it is necessary to abstract the (micro)architectural details and automate the generation and verification of RISC-V microprocessors. The Codasip approach to delivering RISC-V processor IPs is to employ the silicon-proven methodology of the high-level CodAL architecture description language and its suite of tools called Studio to implement various RISC-V microarchitectures. Using Codasip Studio, designers write a high-level description (in CodAL architecture description language) of a processor and then automatically synthesize the design's RTL, testbench, virtual platform models, and processor toolchain (C/C++ compiler, debugger, profiler, etc.). Designers can start using the Codasip processor IPs immediately or, as the Codasip processor IPs are described in CodAL, they can extend the ISA in any way, adding a key differentiator or any other secret sauce into their product.

- **Biografía:**
  Dr. Zdeněk Přikryl is the co-founder and chief technology officer of Codasip GmbH. He has over 10 years of experience in processor design from small MCUs to complex DSPs/VLIWs, along with embedded systems design, HLS, and simulation.